IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) An apparatus comprising:

a plurality of pn-junctions grouped into n(n-1)/2 pairs, wherein each pn-junction pair comprises a first pn-junction coupled antiparallel to a second pn-junction; and

n access points coupled to the plurality of pn-junctions, wherein n is an integer greater than 1;

wherein n-1 pn-junctions are simultaneously accessible via the n access points.

2. (Original) The apparatus of claim 1, wherein one or more of the plurality of pn-junctions are configured to perform temperature measurements.

3. (Original) The apparatus of claim 1, wherein the first pn-junction and the second pn-junction are configured to be accessed independently.

4. (Cancelled)

5. (Original) The apparatus of claim 1, wherein each one of the plurality of pn-junctions is comprised in a respective transistor.

6. (Cancelled)

7. (Currently amended) A method for ~~arranging~~ simultaneously accessing a plurality of pn-junctions, the method comprising:

~~grouping~~ providing an apparatus including the plurality of pn-junctions, wherein the pn-junctions are grouped into n(n-1)/2 pairs, wherein each pn-junction pair comprises a first pn-junction coupled antiparallel to a second pn-junction, wherein the pn-junctions are coupled to n access points, wherein n is an integer greater than 1; and

~~coupling the plurality of pn-junctions to n access points, wherein n is an integer greater than 1~~

accessing n-1 pn-junctions simultaneously via the n access points.

8. (Cancelled)

9. (Original) The method of claim 7, further comprising accessing the first pn-junction and the second pn-junction independently.

10. (Original) A system comprising:

a plurality of pn-junctions grouped into n(n-1)/2 pairs, wherein each pn-junction pair comprises a first pn-junction coupled antiparallel to a second pn-junction, wherein the plurality of pn-junctions are coupled to n access points, wherein n is an integer greater than 1; and

a circuit coupled to the plurality of pn-junctions, wherein the circuit is configured to access n-1 pn-junctions simultaneously via the n access points.

11. (Original) The system of claim 10, wherein the circuit is configured to access one or more of the plurality of pn-junctions to perform temperature measurements.

12. (Original) The system of claim 10, wherein the circuit is configured to access the first pn-junction and the second pn-junction independently.

13. (Original) The system of claim 10, wherein the circuit is configured as a temperature measurement circuit.

14. (Cancelled)

15. (Original) The system of claim 10, wherein each one of the plurality of pn-junctions is comprised in a respective transistor.

16. (Original) The system of claim 15, wherein the circuit is configured to access the respective transistor to perform temperature measurements, wherein in performing the temperature measurements the circuit is operable to provide a first current and a second current to the respective transistor and to determine a change in base-emitter voltage (ΔV_{BE}) of the respective transistor from a first base-emitter voltage (V_{BE1}) corresponding to the first current and a second base-emitter voltage (V_{BE2}) corresponding to the second current.

17. (Cancelled)

18. (Original) A system comprising:

a plurality of pn-junctions grouped into n(n-1)/2 pairs, wherein each pn-junction pair comprises a first pn-junction coupled antiparallel to a second pn-junction, wherein the plurality of pn-junctions are coupled to n access points, wherein n is an integer greater than 1; and

an integrated circuit coupled to the plurality of pn-junctions via the n access points, wherein the integrated circuit is configured to access the first pn-junction and the second pn-junction independently, and wherein the integrated circuit is configured to access n-1 pn-junctions simultaneously via the n access points.

19. (Original) The system of claim 18, wherein the integrated circuit is configured to access one or more of the plurality of pn-junctions to perform temperature measurements.

20. (Original) The system of claim 18, wherein the integrated circuit is configured as a temperature measurement integrated circuit.

21. (Cancelled)

22. (Original) The system of claim 18, wherein each one of the plurality of pn-junctions is comprised in a respective transistor.

23. (Original) The system of claim 22, wherein the integrated circuit is configured to access the respective transistor to perform temperature measurements, wherein in performing the temperature measurements the integrated circuit is operable to provide a first current and a second current to the respective transistor and to determine a change in base-emitter voltage (ΔV_{BE}) of the respective transistor from a first base-emitter voltage (V_{BE1}) corresponding to the first current and a second base-emitter voltage (V_{BE2}) corresponding to the second current.

24. (Original) The system of claim 18, wherein the n access points correspond to n respective pins of the integrated circuit.

25. (Original) The system of claim 19, wherein the plurality of pn-junctions are configured as temperature sensors.

26. (Original) The system of claim 18, wherein the integrated circuit comprises one or more internal pn-junctions configured as temperature sensors to determine a temperature associated with the integrated circuit.

27. (Original) The system of claim 20, wherein the integrated circuit is coupled to a System Management Bus (SMBus).

28. (Cancelled)

29. (New) The system of claim 18, wherein one of the n access points coupled to the integrated circuit is used as a common return point when the integrated circuit simultaneously accesses the n-1 pn-junctions.

30. (New) The system of claim 29, wherein the integrated circuit includes n-1 current sources, wherein each of the n-1 current sources is coupled to the common return point.